2811

AMENDMENT TRANSMITTAL LETTER (Large Entity) Applicant(s): **Adkisson et al.**	Docket No. **BUR919990299 (01240161BA)**

Serial No.	Filing Date	Examiner	Group Art Unit
10/064,171	06/18/2002	T. Magee	2811

Invention: **DOUBLE GATE TRENCH TRANSISTOR**

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated and is transmitted as shown below.

CLAIMS AS AMENDED

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST # PREV. PAID FOR		NUMBER EXTRA CLAIMS PRESENT	RATE	ADDITIONAL FEE
TOTAL CLAIMS	8	-	20	=	0	x $18.00	$0.00
INDEP. CLAIMS	1	-	3	=	0	x $84.00	$0.00
Multiple Dependent Claims (check if applicable) ☐							$0.00
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT							$0.00

- ☒ No additional fee is required for amendment.
- ☐ Please charge Deposit Account No. in the amount of
- ☐ A check in the amount of to cover the filing fee is enclosed.
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  - ☒ Any additional filing fees required under 37 C.F.R. 1.16.
  - ☒ Any patent application processing fees under 37 CFR 1.17.

Marshall M. Curtis

Signature

Dated: **June 27, 2003**

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#43 Amdt SDavis 7/10/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of
James W. Adkisson et al.
Serial No.: 10/064,171 Group Art Unit: 2811
Filed: June 18, 2002 Examiner: T. Magee
For: DOUBLE GATE TRENCH TRANSISTOR

Commissioner for Patents
United States Patent and Trademark Office
P. O. Box 1450
Alexandria, Virginia 22313-1450

AMENDMENT UNDER 37 C. F. R. §1.111

Sir:

In response to the Office Action mailed March 27, 2003, please amend the above-identified application as follows:

In the specification:

Please replace paragraph 0021 with the following paragraph. A marked-up copy thereof showing currently requested changes is provided in the Appendix to this response.

Paragraph 0021:

The SOI wafer, as described above will generally include a thick so-called handling wafer or substrate 10 covered by a buried oxide (BOX) 12. Monocrystalline semiconductor layer 14, in turn, covers the buried oxide 12. Doping levels are relatively low in the preferred embodiment of this device, with the requirement that the channel be fully depleted. Typical doping levels are preferably in the $10^{15}/cm^3$ to $10^{17}/cm^3$ range with the high $10^{16}/cm^3$ range being

preferred. The process of the present invention begins by forming a layer of pad nitride of about 100 nm thickness and a pad oxide of about 3 - 10 nm thickness over the silicon and patterning the nitride using a patterned resist 18. The silicon height will determine device width and is preferably in the range of 50-200 nm. Many suitable resists and lithographic techniques for patterning them are familiar to those skilled in the art and specifics thereof are unimportant to the practice of the invention.

B1 (Contd)

In the claims:

Please substitute the following claim 1 for the like-numbered claim as originally filed. A marked up copy of this claim showing the current changes is attached as an appendix to this amendment.

B2

1. (Amended) A field effect transistor comprising

a conduction channel of sub-lithographic width,

source and drain regions located at opposite ends of said conduction channel, said source and drain regions having silicide sidewalls on a surface thereof, and

polysilicon gate regions on opposing sides of said conduction channel and recessed from said source and drain regions, said polysilicon gate regions having silicide sidewalls formed thereon.

REMARKS

Claims 1 - 8 remain active in this application. Claims 9-17 have previously been canceled. The specification has been reviewed and an editorial revision made where seen to be appropriate. Claim 1 has been amended to improve form. Support for the amendments of the claims is found throughout the application, particularly in Figures 4, 4A, 5 and 5A